tration of the charge barrier n layer **151** is increased in the OFF state, the electric field intensity at this part of the charge barrier n layer **151** becomes high and the breakdown voltage is decreased. The carrier concentration of the charge barrier n layer **151** has an upper limit determined by the breakdown voltage.

[0072] The structure of the embodiment 5 is arranged so as to further increase the upper limit of the carrier concentration of the charge barrier n layer **151** and to further reduce the ON voltage. The feature of FIG. **7** lies in addition of the p layer **152** to FIG. **6** of the embodiment 4.

[0073] With this structure, the depletion layer in the OFF state is extended from an interface between the p layer **152** and the drift n^- layer **110**. Thus, adjustment of the carrier concentration of the p layer **152** enables the breakdown voltage to be surely increased, which leads to the fact that the carrier concentration of the charge barrier n layer **151** can be set at a value higher than the upper limit of the breakdown voltage design of the embodiment 4 and the ON voltage can be reduced.

[0074] The present structure can have effects similar to those of the embodiment 1, and the variation set forth in the embodiment 1 can also have effects similar thereto, with optimum conditions similar thereto. When the structures of the embodiments 2 and 3 are applied to the present structure, the present structure can have effects similar thereto.

Embodiment 6

[0075] FIG. **8** shows a cross-sectional view of a structure in accordance with a sixth embodiment of the present invention. In FIG. **8**, constituent elements having the same reference numerals or symbols as those in FIG. **1** are denoted by the same reference numerals or symbols. In FIG. **8**, reference numeral **602** denotes a resistance.

[0076] FIG. **8** is featured in that the floating p layer **127** in the structure of FIG. **1** is electrically connected to the emitter electrode **600**. As a result, since an increase in the potential of the floating p layer **127** is suppressed, a diode surge voltage of the paired arms upon the IGBT turn-on operation can be adjusted.

[0077] The contact of the floating p layer **127** may be achieved by a direct electrode forming method, through another diffusion layer contacted with the floating p layer **127**, from the peripheral or internal regions of these devices, or continuously or discontinuously in the form of a plurality of contacts. Further when the floating p layer **127** is electrically connected to the emitter electrode **600** via the resistance **602** having a certain size, electric charges passed through the floating p layer **127** can be suppressed from directly going to the emitter electrode **600**, whereby an increase in the charge concentration under the floating p layer **127** as the effect of the present structure can be kept.

[0078] The resistance **602** is not specifically restricted so long as the resistance **602** is a diffusion layer, a built-in resistance of polysilicon or the like, or a resistance such as an externally-connected resistance, to be contacted with the floating p layer **127**.

[0079] FIG. **9** shows a cross-sectional view of a structure in accordance with a sixth embodiment of the present invention. In FIG. **9**, constituent elements having the same reference numerals or symbols as those in FIG. **8** are denoted by the same reference numerals or symbols. In FIG. **9**, reference numeral **603** denotes a floating p layer contact, which is arranged discontinuously.

[0080] In the structure of FIG. **9**, since parts of the floating p layer **127** sufficiently spaced from the floating p layer contacts **603** are connected to the emitter electrode **600** through the resistance per se of the floating p layer **127** proportional to the spaced distance, such effects as mentioned above in connection with FIG. **8** can be obtained. It is advantageous that the effects can be easily designed by adjusting the distance or number of the disconnections of the floating p layer contact **603**.

[0081] FIG. **10** is an embodiment showing a layout of gate termination ends and peripheral breakdown voltage structure in the present invention. In FIG. **10**, constituent elements having the same reference numerals or symbols in FIG. **1** are denoted by the same reference numerals or symbols. In FIG. **10**, reference numeral **128** denotes a p layer.

[0082] A feature of FIG. **10** lies in that the floating p layer **127** is contacted with the p layer **128**, securing a high breakdown voltage even at the termination ends of the trench gates. With this layout, when the p layer **128** is connected to the emitter electrode **600** or connected thereto through a resistance, the potential is fixed. This results in that the breakdown voltage can be made further high with effects similar to those in FIGS. **8** and **9**. In addition, the p layer **128** is made to form an obtuse angle at a contact between the floating p layer **127** and the p layer **128**, the field concentration can also be reduced. The p layer **128** may be made of the same layer as the channel p layer **120**, the floating p layer **127** or a deep p layer for peripheral breakdown voltage structure, or made of a combination of such layers, thus enabling simplification of its process.

[0083] The structures of FIGS. **8**, **9** and **10** can have effects similar to those explained in the embodiment 1. Even for a variation of the embodiment 1 and the optimum conditions thereof, similar effects can be obtained.

Embodiment 7

[0084] FIG. **11** shows a cross-sectional view of a structure in accordance with a seventh embodiment of the present invention. In FIG. **11**, constituent elements having the same reference numerals or symbols as those in FIG. **1** are denoted by the same reference numerals or symbols. In FIG. **11**, reference numeral **140** denotes a semiconductor substrate, and numeral **410** denotes an insulating film (layer).

[0085] FIG. **11** is featured in that the IGBT of FIG. **1** is arranged to form a horizontal type. Even this structure has effects similar to those in the embodiment 1, and a variation of the embodiment 1 or the optimum conditions thereof can have similar effects. When the structures of the embodiments 2 to 6 are applied to the present structure, the present structure can have effects similar thereto.

[0086] In particular, when the present structure is made to be of a horizontal type, a control circuit or a drive circuit therefore can be mounted or integrated, and thus its additional functions can be improved. By utilizing p-n isolation, dielectric isolation, or SOI (Silicon on Insulator) substrate, a parasitic element can be made to be latch-up free, which is advantageous in a functional power converter or the like.

Embodiment 8

[0087] FIG. **12** shows a circuit diagram of a power converter as an eighth embodiment of the present invention. More specifically, FIG. **12** shows an arrangement of an inverter, wherein reference numerals **701** to **706** denote